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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,533	10/12/2000	Motoshi Ito	YAMAP074|US	9029

7590 06/03/2005

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,533	ITO ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23-25 and 27-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23-25 and 27-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/14/2005 has been entered.

Response to Amendment

2. This Office action is in response to the amendment filed 2/14/2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6, 8-21, 23-25 and 27-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis (US PAT. 5,963,970) in view of Kon (6,249,838).

Regarding claim 1, Davis discloses an apparatus for keeping track of erase cycles performed on a plurality of storage blocks in a flash memory comprising the non-volatile memory (10, figure 1), at least one WORD (20, figure 1) of a non-volatile memory, each WORD including a plurality of bits (col. 2 lines 56-63) and information can be erase from the non-volatile memory in a unit of sector, each sector including a plurality of WORDS, and wherein the non-volatile memory comprises an information storage area including at least one WORD in a first sector of the non-volatile memory (col. 4 lines 10-27), and a microprocessor (105, figure 2) for writing pieces of information in a predetermined order in the WORDs of the information storage area (col. 3 line 31 through col. 4 line 10-27). Davis differs from the claimed invention in not specifically teaching for reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, wherein the predetermined permitted updated count is stored in the non-volatile memory in a sector which includes a first program to be executed after reset. However, Kon teaches a data storage unit, i.e., flash memory, comprising a counter initialized to be number of maximum permissible flash memory erasures being stored in a header portion of the flash memory in order to disable further write operation, thereby reading step read out a last piece of information which has been written in the information storage area within maximum permissible flash memory

erasures, wherein the header portion, a sector of the flash memory, includes a boot-up program, i.e., a first program, to be executed after a reset (col. 6 line 36 through col. 7 line 35 and col. 9 line 44 through col. 10 line 28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, wherein the predetermined permitted updated count is stored in the non-volatile memory in a sector which includes a first program to be executed after reset, as per teaching of Kon, in order to improving performance by preventing further write operation.

Regarding claim 2, Davis discloses to erase all of the bits of all of the WORDs in the sector including the information storage area (col. 3 lines 6-12).

Regarding claim 3, Davis discloses to set all the bits of all of the WORDs in each sector to "1" (figure 4 and col. 4 line 42 through col. 5 line 52).

Regarding claim 4, Kon teaches to provide the information storage area in a same sector as an initialization operation program which is a first program to be executed after a reset (figure 3 and col. 7 lines 22-35).

Regarding claim 5, Davis discloses the predetermined order is an ascending order to the address of the WORDs (figure 1).

Regarding claim 6, Kon discloses an upper limit value if the predetermined permitted update count being determined based on the number of WORDs in the information storage area (col. 6 line 63 through col. 7 line 12).

Regarding claims 8-9, Davis teaches to set to a CLEAR state for an erase operation (col. 4 line 66 through col. 5 line 20) so that it recognizes to write at least one write one or more of the plurality of bit in the at least one WORDs from "1" to "0" and the WORDs in the information storage area being searched through in the predetermined order (figure 1-3 and co1.4 lines 13-15). Although Davis does not specifically teaching to read out as the last piece of information, which has been written in the information storage area within the predetermined permitted update count and a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0", Kon teaches a data storage unit, i.e., flash memory, comprising a counter initialized to be number of maximum permissible flash memory erasures being stored in a header portion of the flash memory in order to disable further write operation, thereby reading step read out a last piece of information which has been written in the information storage area within maximum permissible flash memory erasures (col. 6 line 36 through col. 7 line 35 and col. 9 line 44 through col. 10 line 28). Therefore, one of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count and a last hit WORD found in a search through the information storage area for WORDs in which at least one bit is "0", as per teaching of Kon, in order to improving performance by preventing further write operation.

Regarding claim 10, Kon teaches to store the number of times information has been written in the information storage area in an update count storage (abstract and col. 6 lines 63-66).

Regarding claim 11,the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 13, Kon teaches the header area including boot-up program to be executed by the microprocessor unit (col. 7 lines 22-25).

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claims 17-18, the limitations of the claim are rejected as the same reasons set forth in claims 8-9.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 23-24, Kon teaches to read out contents usage count as the number of remaining times or as the number of times the content can be used (col. 7 line 36 through col. 8 line 6).

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 27-28, the limitations of the claims are rejected as the same reasons set forth in claims 23-24.

Regarding claim 29, Davis discloses an apparatus for keeping track of erase cycles performed on a plurality of storage blocks in a flash memory comprising the non-volatile memory (10, figure 1), at least one WORD (20, figure 1) of a non-volatile memory, each WORD including a plurality of bits (col. 2 lines 56-63) and information can be erase from the non-volatile memory in a unit of sector, each sector including a plurality of WORDs, and wherein the non-volatile memory comprises an information storage area including at least one WORD in a first sector of the non-volatile memory (col. 4 lines 10-27), and a microprocessor (105, figure 2) for writing pieces of information in a predetermined order in the WORDs of the information storage area (col. 3 line 31 through col. 4 line 9), wherein the non-volatile unit memory obviously includes a boot area and a system area each including one or more sectors such that the boot area includes an information storage area including at least one WORD and a microprocessor unit initialization program for initializing the microprocessor unit. Davis differs from the claimed invention in not specifically teaching to read out as the last piece of information, which has been written in the information storage area within the predetermined permitted update count, wherein the predetermined permitted updated count is stored in the non-

volatile memory in a sector which includes a first program to be executed after reset. However, Kon teaches a data storage unit, i.e., flash memory, comprising a counter initialized to be number of maximum permissible flash memory erasures being stored in a header portion of the flash memory in order to disable further write operation, thereby reading step read out a last piece of information which has been written in the information storage area within maximum permissible flash memory erasures, wherein the header portion, a sector of the flash memory, includes a boot-up program, i.e., a first program, to be executed after a reset (col. 6 line 36 through col. 7 line 35 and col. 9 line 44 through col. 10 line 28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Davis in reading out a last piece of information which has been written in the at least one WORD of the information storage area within a predetermined permitted update count, wherein the predetermined permitted updated count is stored in the non-volatile memory in a sector which includes a first program to be executed after reset, as per teaching of Kon, in order to improving performance by preventing further write operation.

Regarding claim 30, Davis teaches the memory having support software to control the setting within the information storage area (col. 3 line 64 through col. 4 line 3) so that the boot area obviously comprises a check program for checking contents of the information storage area, as well as Kon (col. 7 lines 22-35).

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in clam 4.

Regarding claim 32, Davis discloses the boot area further comprises I/F control means for receiving a program to be stored in the system area from an upper control unit which is

connected to the information update count managing apparatus (figure 3), as well as Kon (col. 7 lines 22-25).

Regarding claim 33, Davis discloses flash memory update means (245, figure 3) for updating a program in the system area.

Regarding claim 34, Kon teaches the microprocessor unit executing the microprocessor unit initialization program, and then waits for reception from the upper control unit, which is connected to the information update count managing apparatus immediately after the micro processor unit is reset (col. 7 lines 22-59).

Regarding claim 35, Davis discloses the microprocessor unit calls a program in the boot area from a program in the system area (col. 5 line 53 through col. 6 line 6), as well as Kon (col. 7 lines 22-25).

Regarding claim 36, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 37, the limitations of the claim are rejected as the same reasons set forth in claims 3 and 8-9.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis (US PAT. 5,963,970) in view of Kon (6,249,838) as applied to claim 1 above, and further in view of Sawabe (US PAT. 6,122,434).

The combination of Davis and Kon differs from the claimed invention in not specifically teaching the pieces of information include regional information, which is used for controlling a region where content can be reproduced. However, Sawabe an information recording medium

including regional information, which is used for controlling a region where content can be reproduced (col. 2 line 9 through col. 4 line 35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Davis and Kon in having the pieces of information include regional information which is used for controlling a region where a content can be reproduced, as per teaching of Sawabe, because it makes user friendly by reproducing an identical disk in different ways according to predetermined levels which are set differently in various countries.

Response to Arguments

6. Applicant's arguments with respect to claims 1-21, 23-25 and 27-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lampson et al. (US 2003/0196110) dislcoses boot blocks for software in a computer system having an atomic operation to set an identity of a piece of software into the software identity register (abstract). Doller (US PAT. 5,621,687) discloses a method for controlling the programming and erasure time of a non-volatile memory array in a memory device (abstract). Robinson et al. (US PAT. 5,544,356) discloses block-erasable non-volatile semiconductor memory, which tracks and stores the total number of write/erase cycles for each block (col. 4 lines 14-49).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is (571) 272-4183. The examiner can normally be reached on Tue-Fri 8:30 AM-6:00 PM, and alternate Monday 8:30 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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